REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated May 25, 2007 (U.S. Patent Office Paper No. 20070523). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 1-3 and 5-16 stand for consideration in this application, wherein claim 4 is being canceled without prejudice or disclaimer, while claims 1, 6 and 14 are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention.

Additional Amendments

The specification and drawings are being amended to correct formal errors and to better disclose and describe the features of the present invention as claimed. All amendments to the application are fully supported therein, as discussed more fully hereinbelow. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Formal Objections or Rejections

The Examiner objected to the Title of the Invention as being non-descriptive, and objected to Figs. 3-6 and 15 for lacking a legend of "Prior Art."

The Examiner rejected claims 1-5 under 35 U.S.C. §112, first paragraph, as failing to comply with the written description requirement.

As outlined above, the drawings Title of the Invention and the drawings are being amended to correct the formal errors identified by the Examiner. Further, the claims are being amended to correct formal errors and to more particularly point out and distinctly claim the subject invention. As such, Applicants will submit that the above-noted formal objections and rejections are hereby obviated.

Prior Art Rejections

The Examiner rejected claims 6-9 under 35 U.S.C. §102(b) as being anticipated by Morishita et al.(US 5,396,480). Under 35 U.S.C. §103 (a), the Examiner rejected: (1) claims 10-13 as being unpatentable over Morishita '480; (2) claims 14-16 as being unpatentable over Morishita '480 in view of Kimura (US 5,905,695); and (3) claims 1-5 as being unpatentable over Morishita '480 in view of Abe et al. (US 6,801,240). Applicants have reviewed the above-outlined rejections, and hereby respectfully traverse.

The present invention as recited in claim 1 is directed to an information recording method for recording information on an information recording media by means of light or magnetism, comprising the steps of: converting an encoded data into m pieces of parallel data bits; inputting m pieces of data bits as an input signal to a multiplexing circuit to which m pieces of data bits are input and which outputs n pieces of data bits (hereinafter referred to as an m:n multiplexer), where $m>n\geq 2$; synchronizing the n pieces of output data bits by obtaining a clock used for multiplexing the m pieces of input data bits into the n pieces of output data bits from a single generating source, and outputting n pieces of data bits from the m:n multiplexer at a speed greater than that of the input signal; and recording information with the n pieces of data bits.

As recited in claim 6, the present invention is directed to an information recording equipment comprising: an encoding circuit which encodes data to be recorded; a recording pulse shaping circuit to which output of said encoding circuit is input and which outputs m pieces of pulse signals as parallel signals; an m:n multiplexer which multiplexes the m pieces of pulse signals output from said recording pulse shaping circuit and outputs n pieces of pulse signals, where $m>n\geq 2$; a laser driver circuit which is driven by the n pieces of output signals from said m:n multiplexer; and a laser beam source which is driven by output of said laser driver circuit, wherein the m:n multiplexer synchronizes the n nieces of output data bits by obtaining a clock used for multiplexing the m pieces of input data bits into the n pieces of output data bits from a single generating source.

Further, the present invention as recited in claim 14 is directed to an evaluation equipment comprising: an encoding circuit which encodes test data; a recording pulse shaping circuit to which output of said encoding circuit is input and which outputs m pieces of pulse signals as parallel signals; an m:n multiplexer which multiplexes the m pieces of pulse signals output from said recording pulse shaping circuit and outputs n pieces of pulse signals, where

m>n≥2; a laser driver circuit which is driven by the n pieces of output signals from said m:n multiplexer; a laser beam source which is driven by output of said laser driver circuit; and a control circuit unit which controls operation, using said test data, wherein the m:n multiplexer synchronizes the n pieces of pulse signals by obtaining a clock for multiplexing the m pieces of pulse signals into the n pieces of pulse signals from a single generating source. Support for the invention as claimed may be found throughout the specification, including but not limited to page 10, line 5 to page 12, line 7

Among the features of the present invention, (a) encoded data is converted into m pieces of data bits that are outputted in parallel; (b) the m pieces of data bits are inputted to an m:n multiplexer as an input signal, to which m pieces of data bits are input and which outputs n pieces of data bits (m>n≥2); and (c) the clock used for the multiplexing of the m pieces of input data bits into the n pieces of output data bits is obtained from a single generating source, so that the n pieces of output data bits can be synchronized and the n pieces of data bits can be outputted from the m:n multiplexer at a speed greater than that of the input signal.

Feature (a) is implemented in a recording pulse forming circuit, while feature (b) is implemented in an m:n multiplexer, as recited in at least claims 1, 6 and 14. The present invention achieves the objects of the invention set forth in the specification on page 3, line 9 to page 4, line 15, and thereby makes it possible to handle high-speed recording while maintaining the time accuracy of a plurality of laser pulses based on which a write strategy is formulated.

For example, with reference to the specification on Embodiment 1 involving a 4:2 multiplexer, as described on page 11, lines 3-15, the 4:2 multiplexer can output a data signal at twice the speed of the input, whereby the pulse position accuracy can also be increased by two-fold (*"In view of the m:n multiplexer feature, input signal data bits are supplied at a lower speed by n/m than the output signals and, accordingly, a low-speed data input interface with reduced loss and crosstalk is applied and packaging is easy. By increasing the number of m, the number of parallel input data signals increases and data can be input at a still lower speed,"* see page 13, lines 1 -7).

In contrast to the present invention, Morishita '480 merely discloses in Fig. 3 that channel data is inputted to a timing pulse generator 51 from which timing signals WS1 to WS4 with their individual recording levels are sequentially outputted as shown in Fig. 4(b), wherein switches 53 to 56 are selectively switched by a multiplexer 52 depending on the inputted timing signals WS1

to WS4 and a laser is driven by an output waveform shown in Fig. 4(a). Applicants will contend that the above-described structure and operation of Morishita '480 cannot and do not embody or achieve the aforementioned Features (a), (b), or (c).

Specifically, the timing pulse generator 51 of Morishita '480 merely outputs the timing signals WS1 to WS4 sequentially as shown in Fig. 6(b) in accordance with the inputted channel data. At best, this corresponds to the LD driver circuit 15 of the present invention shown in Fig. 1, and is NOT an m:n multiplexer to which m pieces of data bits arc inputted and which outputs n pieces of data bits. Further, the multiplexer 52 of Morishita '480 does not synchronize the n pieces of output data bits by obtaining the clock for multiplexing from a single generating source, nor does it output n pieces of data bits at a speed greater than the input signal.

As such, at the very least, Morishita '480 cannot anticipate any structure or operation that embodies synchronizing the n pieces of output data bits by obtaining a clock used for multiplexing the m pieces of input data bits into the n pieces of output data bits from a single generating source, and outputting n pieces of data bits from the m:n multiplexer at a speed greater than that of the input signal, wherein encoded data is converted into m pieces of data bits that are outputted in parallel, as in the present invention as claimed. The present invention is distinguishable from Morishita '480.

The secondary references of Abe and Kimura were only cited for showing general features that the Examiner noted as being absent from Morishita '480. However, while Abe '240 and Kimura '695 apply multiple levels of data in magnetic disc apparatuses, the structures of their multiplexers differ from that of the present invention. Neither reference provides any disclosure, teaching or suggestion that makes up for the deficiencies in Morishita '480 as described above, such that their combinations could now embody each and every feature of the present invention as claimed. Rather, even if all three references were combined, Applicants will contend that those combinations would still lack, among other features, the combination of elements of the present invention that included synchronizing the n pieces of output data bits by obtaining a clock used for multiplexing the m pieces of input data bits into the n pieces of output data bits from a single generating source, and/or outputting n pieces of data bits from the m:n multiplexer at a speed greater than that of the input signal. Consequently, the present invention would not have been obvious to one of ordinary skill in the art given prior art cited, either

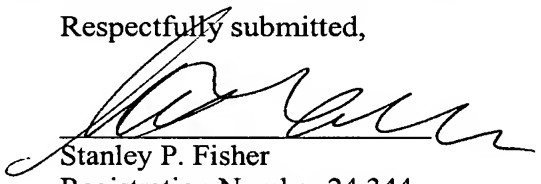
individually or in combination. The present invention as a whole is distinguishable and thereby allowable over the prior art of record.

Conclusion

In view of all the above, Applicant respectfully submits that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,



Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

August 20, 2007

IN THE DRAWINGS:

Please approve the changes to the drawings as outlined in the attached Letter to the Draftsperson, and as shown in the accompanying revised replacement drawings. Specifically, Figures 3-6 and 15 are being marked with the legend "PRIOR ART".